AMENDMENTS TO THE SPECIFICATION

Please amend these paragraphs of the specification as indicated:

Page 1, lines 6-8

This invention is a Continuation-in-Part of ~~pending~~ U.S. Patent Application No. 09/179,137, "Virtualization System Including a Virtual Machine Monitor for a Computer with a Segmented Architecture," filed 26 October 1998, which issued as U.S. Patent No. 6,397,242 on 28 May 2002.

Page 8, line 25, to page 26, line 4

Figure 2 shows the system configuration in a preferred embodiment of the invention. In this preferred embodiment, the intermediate software comprises two main components -- an operating system 230, which includes the drivers 130, and a virtual machine monitor (VMM) 250, which includes the exception handler 134 and the binary translator 136. In this embodiment of the invention, the VMM 250 is thus at the same system level as the operating system 230 itself, with both communicating directly with the hardware 100. This configuration, as well as its advantages, are described in ~~the co-pending~~ U.S. Patent No. 6,397,242 ~~Application Serial No. 09/179,137, "Virtualization System Including a Virtual Machine Monitor for a Computer with a Segmented Architecture," filed 26 October 1998, which is incorporated herein by reference~~.

Page 10, lines 15-26

In some implementations of the invention, binary translation may be used to convert every source instruction into at least one corresponding target instruction. This is a common solution, but every binary translation of a source instruction that could have been executed directly by the hardware causes a delay that could theoretically be avoided. U.S. Patent ~~Application~~ No. 6,397,242 ~~09/179,137~~ discloses a system and a method for virtualizing a computer that in fact avoids this delay by implementing both binary translation and direct execution within a single virtual machine monitor, as well as

a mechanism for switching to binary translation only when direct execution is not possible. Specifically, it runs the virtual operating system with reduced privileges so that the effect of any instruction sequence is guaranteed to be contained in the virtual machine. Because of this, the VMM must handle only the traps that result from attempts by the virtual machine to issue privileged instructions.

Page 10, line 27, to page 11, line 2

This invention involves an improvement in a binary translator, and as such does not depend on the use of a virtual machine monitor or other intermediate software that allows both binary translation and direct execution; nonetheless, this invention is particularly advantageous when used in the binary translator described in U.S. Patent ~~Application~~ No. 6,397,242 ~~09/179,137~~, since it provides even greater speed with precise exception handling.

Page 11, line 26, to page 12, line 8

See Figure 3. There are three main portions of the VMM 250 according to the preferred embodiment of the invention: a binary translation execution engine 300, a direct execution execution engine 302, and a decision sub-system 304 that determines which execution mode to use. The concepts and general techniques of binary translation and direct execution are well known in the art. As is mentioned above, in the preferred embodiment of the invention, however, the VMM 250 incorporates *both* execution modes, as well as the decision sub-system 304, which selects between the two. This invention is directly primarily to the binary translator 136 ~~300~~; accordingly, most of the following discussion involves this sub-system. Furthermore, the details of the dual execution-mode operation of the VMM 250 used in the preferred embodiment of the invention are laid out in U.S. Patent ~~Application~~ No. 6,397,242 ~~09/179,137~~. Nonetheless, for completeness, the main components of both execution sub-systems, and the preferred mechanism for switching between them, are briefly discussed here.

Page 14, lines 13-26

The memory tracing mechanism implemented in the preferred embodiment of the invention is described in detail in U.S. Patent ~~Application~~ No. 6,397,242 ~~09/179,137, "Virtualization System Including a Virtual Machine Monitor for a Computer with a Segmented Architecture," which is incorporated here by reference~~. The memory tracing mechanism described in that application uses a combination of the processor's memory management unit (MMU) 116, via page faults, and the ability, using either hardware or software (in particular, the binary-translation sub-system) to execute instructions one-by-one, that is, to single-step the virtual machine. The memory tracing mechanism can be implemented on top of the mechanism that virtualizes the physical address space of the virtual machine. This latter mechanism is present in conventional virtual machine monitors that support multiple virtual machines and can be implemented using known techniques. In the preferred embodiment of the invention, it is implemented by having the VMM manage the MMU through an address space separate from the one managed by the VM.

Page 21, lines 1-8

As is mentioned above, the three components of the preferred embodiment of the invention that allow co-location of the VMM 250 with an unmodified host operating system 230. The details of these components are described in U.S. Patent ~~Application~~ No. 6,496,847 ~~09/151,175~~ ("System and Method for Virtualizing Computer Systems"), issued 17 December 2002 ~~filed 10 September 1998~~. Although this configuration is not essential to the implementation and use of this invention, it is preferred since it avoids the delay and complication inherent in requiring the VMM to drive devices for which the host operating system already has efficient drivers. The key features of this arrangement are: